CIRCUIT FOR ELECTROSTATIC DISCHARGE PROTECTION

Technical Field

The present invention relates to a circuit for protection against an electrostatic discharge (ESD) event. In particular the invention is applicable to protection of internal elements of integrated circuits (IC).

Background of the invention

Semiconductor devices, and especially integrated circuits, are very sensitive to BSD events that can cause serious degradation or damage of the IC. Solutions known in the art that protect internal elements of the IC from damage are based on circuits that shunt the ESD current between the IC power supply rails.

One of the circuits known in the art protects a power supply rail from positive ESD events referenced to a grounded power supply rail. The circuit consist of a trigger circuit, an inverter stage, and a large NMOSFET transistor. Trigger circuit is designed as a resistor-capacitor (RC) transient detector. In response to an ESD event that induces a rapid positive voltage transient on the power supply rail, trigger circuit initially holds a middle node of RC trigger circuit well below grounded power supply rail. The inverter stage then drives the gate of NMOSFET. Once turned on, NMOSFET transistor provides a low resistance shunt between the power rail and the grounded rail. NMOSFET transistor will remain conductive for a period of time, which is determined by the RC time constant of the trigger circuit. It is critical that this RC time constant is long enough to exceed the maximum expected duration of an ESD event, typically a few hundred nanoseconds, while short enough to avoid false triggering of the clamp circuit during normal ramp-up of the power

rail, typically a few milliseconds. During normal operation of the IC, with a constant power supply level, NMOSFET is biased in a nonconductive state.

Since the resistor in the RC chain is NWELL resistor and the capacitor is MOS capacitor the described circuit has a number of disadvantages including the following:

- huge size of the NWELL resistor,
- temperature dependency of resistance of NWELL resistor, which results in false triggering of the circuit.

Attempts at replacing NWELL resistor with smaller PMOSFET have failed since they could not exclude false clamp triggering in power up conditions. Up to 0.5V (threshold of PMOSFET) on power supply rail the PMOSFET does not conduct and voltage at middle node of RC chain does not rise and the threshold of the inverter in the clamp preamplifier exceeds voltage at middle node of RC trigger circuit for time enough for false clamp triggering.

Hence, considering the above disadvantages, an improved circuit for ESD protection is needed. The new circuit should be smaller and more reliable.

Summary of the Invention

There is a need for a circuit for electrostatic discharge protection, which alleviates or overcome the problems of the prior art.

The circuit according to the invention is preferably for use in protection of integrated circuits.

A circuit providing protection against electrostatic discharge (ESD) for internal elements of an Integrated Circuit (IC) in accordance with the present invention is connected to a power rail and a ground rail and to an inverter of a clamp preamplifier. Said circuit comprises a PMOSFET resistor with a gate connected to said ground rail,

a drain connected to said inverter's (INV) input node, a source and a bulk connected to said power rail. An NMOSFET capacitor of the protection circuit has a gate connected to said inverter input node, a drain, a source and a bulk connected to said ground rail. The protection circuit also comprises a PMOSFET capacitor with a gate connected to said inverter input node (ESD_RC), a drain, a source connected to said ground rail and a bulk connected to said power rail.

The advantage of the present invention is that the area occupied by ESD protection circuit is about 5 times less in comparison to the circuits known in the art. As a result of introducing small PMOSFET resistor also the capacitor can be done smaller. Furthermore, including PMOSFET resistor significantly reduces the temperature dependency of the circuit.

Brief description of the drawings

The present invention will be understood and appreciated more fully from the following detailed description taken in conjunction with the drawings in which:

Fig.1 is schematic diagram illustrating a circuit for protection against an ESD event in accordance with an embodiment of the invention,

Fig.2 illustrates transient response of the circuit in Fig.1 for low VDD slew rate (3V/μs),

Fig.3 illustrates transient response of the circuit in Fig.1 for high VDD slew rate (300V/μs).

Detailed description of the preferred embodiment

Referring to Fig.1 a circuit providing protection against electrostatic discharge (ESD) for internal elements of an Integrated Circuit (IC) according to the present invention is connected to a power rail VDD and a ground

rail VSS and to an inverter INV of a clamp preamplifier. The protection circuit comprises a PMOSFET resistor R with a gate connected to said ground rail VSS, a drain connected to said inverter's INV input node ESD_RC, a source and a bulk connected to said power rail VDD. The circuit also comprises an NMOSFET capacitor C1 with a gate connected to said inverter's INV input node ESD_RC, a drain, a source and a bulk connected to said ground rail VSS, and a PMOSFET capacitor C2 with a gate connected to said inverter's INV input node ESD_RC, a drain, a source connected to said ground rail VSS and a bulk connected to said power rail VDD.

In another embodiment of the present invention the NMOSFET capacitor C1 has a non-linear characteristic.

In yet another embodiment of the present invention the PMOSFET capacitor C2 has a non-linear characteristic.

In most preferable embodiment both capacitors, C1 and C2, have non-linear characteristics.

In another embodiment of the present invention a ratio of capacitance of said PMOSFET capacitor C2 to capacitance of said NMOSFET capacitor C1 decreases when voltage at said power rail VDD exceeds NMOSFET threshold (-0.5V).

Reference is now made to Fig.2, which depicts transient response of the circuit according to the present invention in power up conditions (VDD slew rate = 3V/μs). Transient response of the RC chain at ESD_RC node begins to rise immediately with VDD rising. The PMOSFET capacitor C2 helps to charge the NMOSFET capacitor C1 and to pull up voltage at ESD_RC node over voltage at INV_TH node at the beginning of power on. This allows avoiding false clamp triggering during power up. When the ESD_RC slew rate reaches the slew rate of VDD the PMOSFET capacitor C2 does not further impact on transient response.

Reference is now made to Fig.3, which illustrates transient response of the circuit according to the present invention during an ESD event (VDD slew rate = 300 V/μs). Transient response of the RC chain at ESD_RC node begins to rise slower then VDD voltage and the voltage at INV_TH node exceeds ESD_RC voltage causing correct clamp triggering.

The circuit in accordance with the invention may be used in various electronic devices, in particular it can be an integral part of integrated circuits.

It will be understood that the invention tends to provide the following advantages singly or in any combination:

- significant reduction of space required for the resistor and capacitor in RC chain and in consequence for the circuit,
- less temperature dependency of the circuit due to excluding NWELL resistor,
- increased reliability caused by elimination of false triggering during power up.